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Design and Implementation of CMOS 64-Bit Comparator Using Different Technologies

Kanika Hans[1], Amandeepkaur Dhaliwal[2]

[1]Student, M.Tech ECE, Punjabi University Patiala
[2]Asst Professor, ECE, Punjabi University Patiala

Abstract: **we represent a high speed and average power consumption 64-Bit Comparator using CMOS technology. Comparison is most basic arithmetic operation that compares one number is greater than, less than or equal to. Comparator is used for comparison operation. Comparison between these different technology is calculated by simulation that is performed at different technologies in Tanner EDA tool.**

Keywords: **N-Bit Comparator, delay, power consumption.**

I. INTRODUCTION

A circuit that compares two binary numbers and decides whether they are equal or not is called comparator. Comparator is a combinational circuit that compares two binary numbers and determine their relative magnitude and decides which number is greater , smaller or both are equal. Comparison between two binary numbers is widely used in computer systems and devices. The current mode signal processing using CMOS technology has gained great interest in circuit designing. With increasing in demand of high speed and low power application, the current-mode circuit has been considered to be an alternative to voltage-mode circuit.It is desirable that comparators must provide high speed and low power consumption. In this we need to design such kind of a comparator which compares the value of two 64-bit numbers and output X becomes to 1(high) when the first number A is larger than the second number B, output Y becomes to 1(high) when the two numbers A and B are equal otherwise both are not active Our method is to extend the 1-bit comparator to an 8-bit comparator by connecting 1-bit's eight comparator in series. Similarly, 64-bit comparator is also obtained by connecting eight 8-bit comparator's in series. The basic block diagram for N-bit magnitude comparator is as given[2]:-

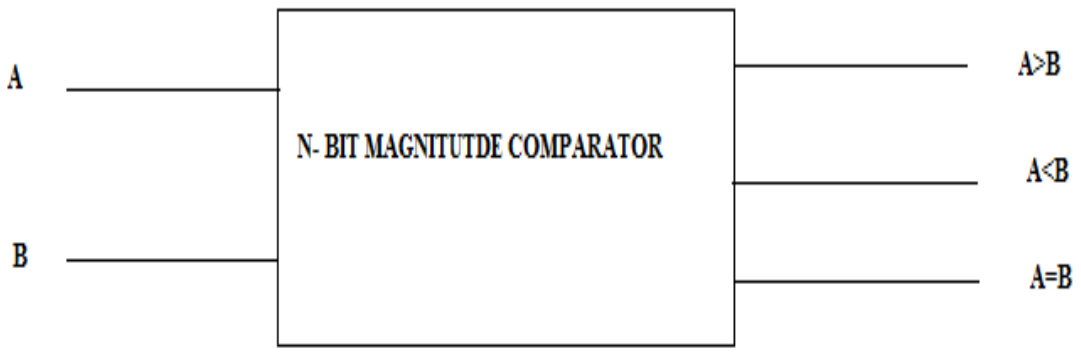

Fig- 1.1 Block Diagram of N-BIT MAGNITUDE COMPARATOR [2]

II. CMOS TECHNOLOGY

It consists of one NMOS & one PMOS transistor. If input A=0 (logic low) then both gates are at zero potential & PMOS is ON & provide low impedance path from VDD to output (Y). Therefore output (Y) approaches to high level of VDD. If input A=1 (logic high) then both gates are at higher potential but NMOS is ON & provide low impedance path between ground & output (Y). Therefore, output (Y) approaches to low level of 0V. Pull up network has only PMOS circuitry & Pull down network has only NMOS circuitry. The function of PUN is to provide connection between output & VDD The function of PDN is to provide connection between output & GND. PUN and PDN networks are constructed in a way that one & only one network is conducting at a time. Number of transistors for N-input logic gate is 2N. Any logic function can be realized by NMOS pull-down and PMOS pull-up network .Gates are very simple. The basic gate is an inverter, which is only two transistors. This together with the low power means it lends itself well to dense integration. Or conversely get a lot of logic for the size, cost and power. low power consumption .High degree of noise immunity. High input impedance.With increasing demand of high speed and low power application the transmission gate can preferred over the CMOS transistor. Transmission gate comparator design has required less number of MOSFETS comparison then CMOS. So the feature size and cost of device can be reduced. It is used in analog to digital converters, oscillators, current to frequency converters, VLSI neural network, sensor circuit and portable wireless communication etc. Proposed the first high speed, low input impedance current comparator using a simple inverter. Tarff's approach has been modified by a number of designs, where speed increases have been attained at the cost of increasing power consumption. It is desirable that comparators must provide high speed and low power consumption. Here we design such kind of a comparator which compares the value of two 4-bit numbers and output X becomes to 1 when the two numbers A and B are equal, output Y becomes to 1 when the first number[3]. Another Type of The Magnitude comparator is a device which facilitates the comparison of two numbers.

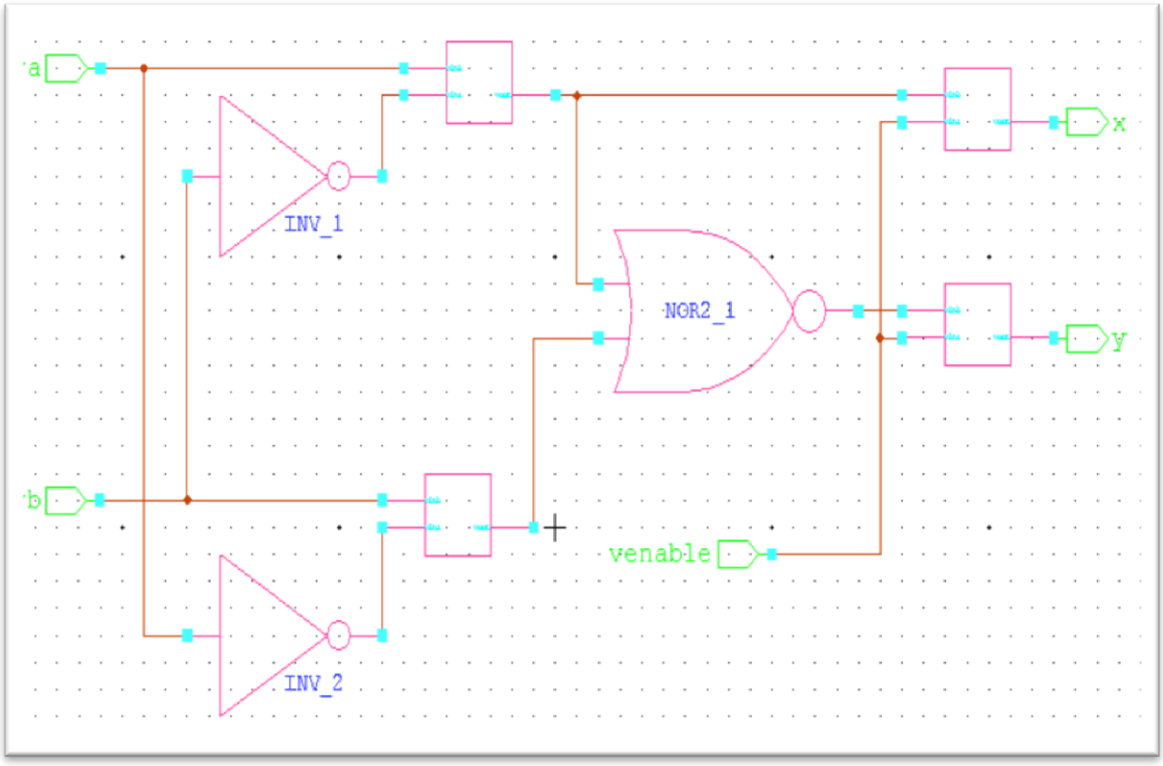

Fig 1.2 One-Bit Comparator[2]

A comparator's basic logic diagram can be implemented in various ways ranging from easy to complex, power consuming to power efficient, high transistor count to very low transistor count and a wide range of power delay product statistics. The high performance techniques being employed in different VLSI circuits aim to reduce the power, delay, PDP (Power Delay Product) and area. The different logic styles implemented in this paper exhibit different performance characteristics. Based on the comparative analysis, we have chalked out the best and worst styles based upon their estimated power consumption, PDP and the area calculation based upon the number of transistors

I. 64-Bit Comparator using 65nm technology

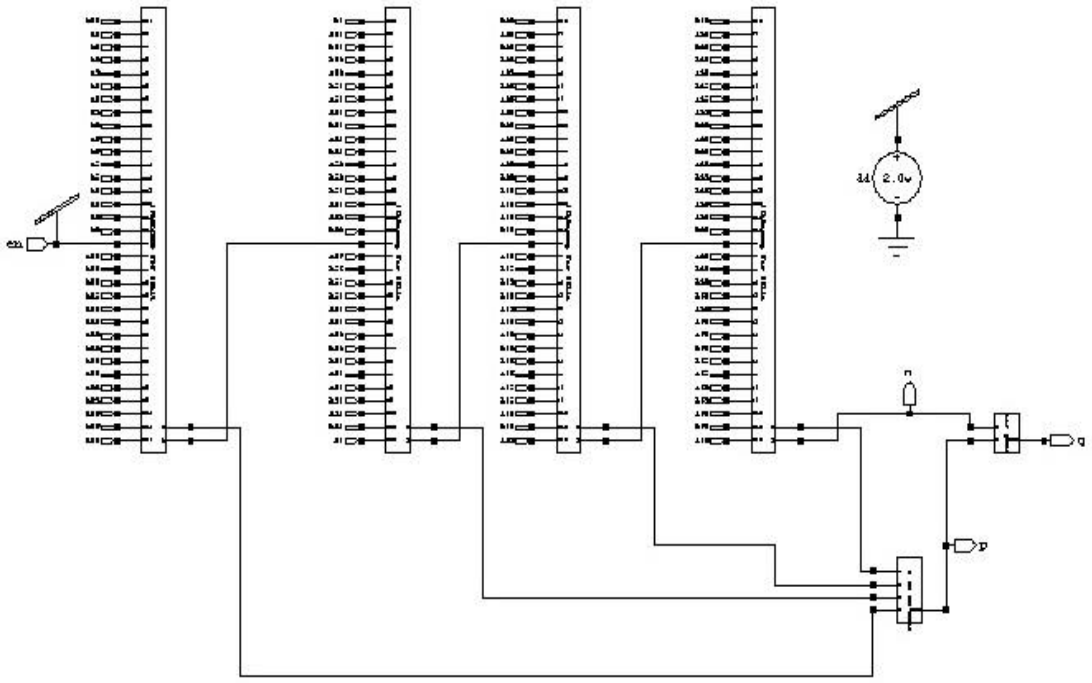

Fig 1.3 64- Bit Comparator

64-Bit comparator consisting of four 16- bit comparator placed in series consisting one nor gate and one 4 Bit And gate. This Comparator is having four inputs a1,b1,a2,b2,a3,b3,a4,b4,and so on up to a64,b64, and three outputs P(A>B),Q(A<B),R(A=B). This Comparator is Designed and operated at 2v in 65nm technology where length of each NMOS(L=65nm,W=120nm) and PMOS(L=65,W=240) is taken

II. 64-Bit Comparator using 45nm technology

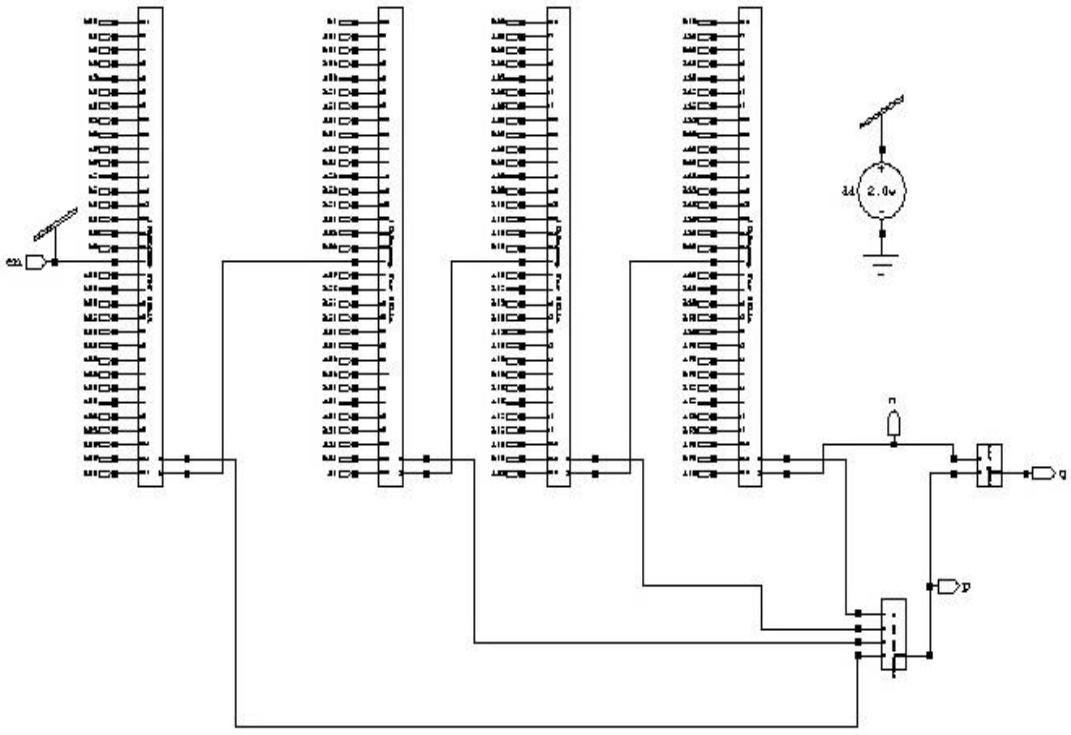

Fig1.464-Bit Comparator

64-Bit Comparator of four 16-Bit comparator placed in series consisting one NOR gate and one 4-Bit AND gate. This Comparator is having four inputs a1,b1,a2,b2,a3,b3,a4,b4 and so on a64,b64 and three outputs P(A>B), Q(A=B),R(A<B). This comparator is designed and operated at 1v in 45nm technology where length of each NMOS (L=45nm,W=80nm) and PMOS(L=45nm,W=160nm). This circuitry is designed using Tanner Tool, S-edit-Spice, and W-edit

Table I: - Performance Parameters of 64-Bit Comparator using 45nm Technology

Comparator	Average power consumption (µwatt)	Delay (ns)	PDP (Fwatt-sec)
1-Bit Comparator	2.88	2.48	6.72
4-Bit Comparator	9.50	2.64	24.72
16-Bit Comparator	50.7	2.31	11.75
64-Bit Comparator	4.62	2.05	9.55

Table II: - Performance Parameters of 64-Bit Comparator using 65nm Technology

Comparator	Average power consumption (µwatt)	Delay (ns)	PDP (Fwatt-sec)
1-Bit Comparator	20.4	2.05	41.8
4-Bit Comparator	10.98	6.03	65.7
16-Bit Comparator	90.4	5.99	54.1
64-Bit Comparator	4.64	6.18	28.6

Table III: - Performance Parameters of 64-Bit Comparator using 180nm Technology

Comparator	Average power consumption (µwatt)	Delay (ns)	PDP (Fwatt-sec)
1-Bit Comparator	24.4	3.99	97.3
4-Bit Comparator	87.2	4.28	373.2
16-Bit Comparator	116.2	4.26	495
64-Bit Comparator	85	2.30	195.5

III. Comparison Graphs for 64 Bit Comparator at 65nm and 45nm Technology with previous work:-

III.1 Delay Graph:-

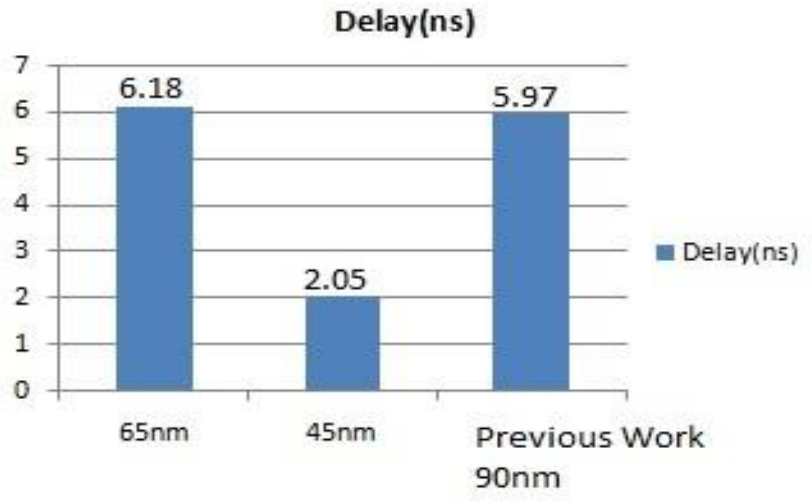

Fig 1.5 PDP parameters for 64 Bit Comparator at Different Technologies

III.2 Average Power Consumption Graph:-

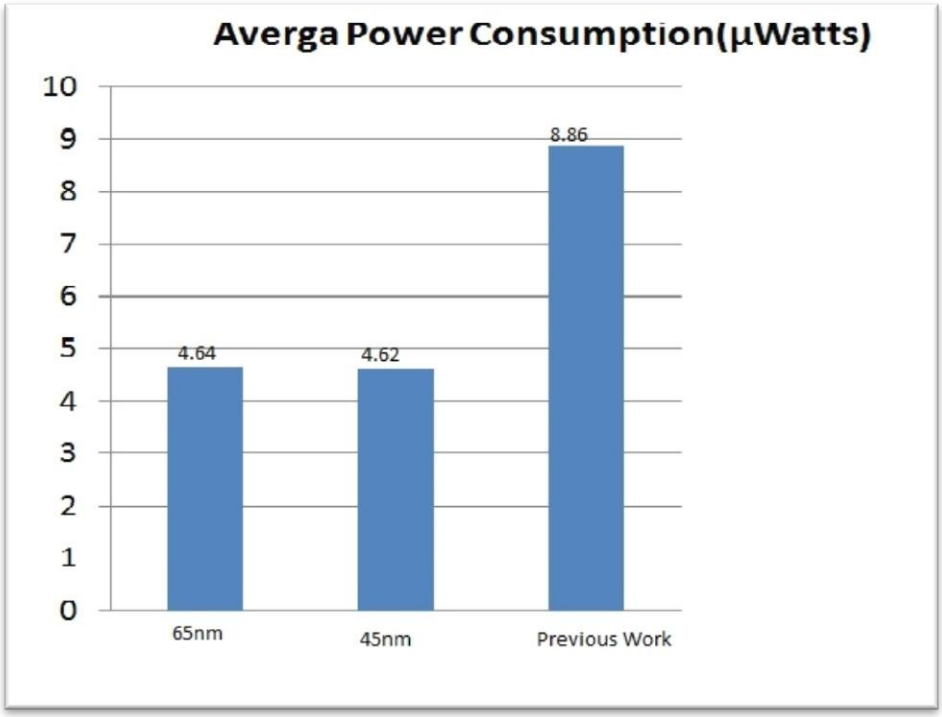

Fig 1.6:- PDP parameters for 64 Bit Comparator at Different Technologies

III.3 Power Delay Product Graph:-

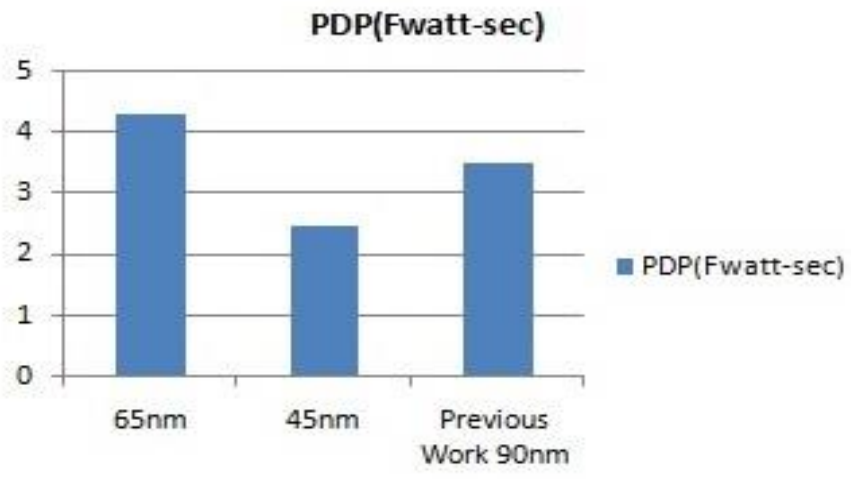

Fig 1.7:- PDP parameters for 64 Bit Comparator at Different Technologies

III. CONCLUSION

64-Bit Comparator has been realized using two different technologies 65 nm and 45 nm. Their comparative analysis has been realized with 90 nm technology previous work. The proposed circuit compared to Conventional 64 Bit Comparator, provides a considerable reduce in 4µwatt at the input voltage of 2v for 65 nm technology and a considerable reduce in 4.2µwatt at the input voltage of 1v for 45 nm technology. Optimizing transistor size plays a very important role in design of CMOS logic circuits. In this design we have focused on keeping optimum design for low power applications. For input voltage greater than or equal to 0.8V, the proposed circuit gives reduction in delay and average power consumption. A

considerable amount of 4µwatt reduction in the output voltage values a lot in power energy scavenging applications. The Comparator circuit operates reliably and provides three outputs P(A>B), Q(A=B), R(A<B). The proposed circuit only consumes 4.62µW at input voltage of 1 v and 4.64µW at input voltage of 2v at 65nm technology.

REFERENCES

[1] Geetanjali Sharma, Hiten Arora, Jitesh Chawla, and Juhi Ramzai "Comparative Analysis of a 2-Bit Magnitude Comparator using various High Performance Techniques", IEEE CCSP 2015 conference.

[2] Anjuli, Satyajit Anand "High Performance 64-Bit Binary Comparator", 2014 International Conference on Reliability, Optimization and Information Technology IEEE 2014.

[3] M.Amala, "Design of Low Power 12-Bit Magnitude Comparator", IJTEL, 2013.

[4] Madhina Basha "Transistor Implementation of reversible Comparator Circuit using Low Power Technique", IEEE 2012.

[5] A N Nagamani , H R Bhagyalakshmi , " Novel Low Power Comparator Design using Reversible Logic Gates " Indian Journal of Computer Science and Engineering ,2011.

[6] F.Frustaci, Corsonello, "A new low power high-speed single –clock-cycle binary Comparator," IEEE 2010.

[7] K. Banerjee, "A novel variation tolerant keeper architecture for high –performance low –power wide fanin dynamic or gates" IEEE 2010.